UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,164	01/26/2004	Chan-Suk Lee	2557-000200/US	6719

30593 7590 07/01/2005

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,164	LEE, CHAN-SUK	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/763164 Attorney's Docket #: 2557-000200/US
Filing Date: 1/26/2004; claimed foreign priority to 2/20/2003

Applicant: Lee

Examiner: Alexander Williams

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6-8, 16, 17, 19 and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Haba et al. (U.S. Patent # 6,376,904 B1).

1. Haba et al. (figures 1 to 14) specifically figure 9 show a stacked semiconductor package **900** comprising: a first semiconductor chip **(10d or 910a)**; a second semiconductor chip **(950 or 910b)** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; and at least one first conductor **(wire electrically connecting 910d to 950 but not labeled)** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip.

2. The package of claim 1, Haba et al. show wherein the first conductor electrically connects at least one bond pad **(pad on 910d but not labeled)** on the first semiconductor chip with at least one bond pad **(pad on 950 but not labeled)** on the second semiconductor chip.

6. The package of claim 1, Haba et al. show wherein a plurality of first conductors electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Haba et al. further comprising: the plurality of first conductors respectively electrically connecting a plurality of bond pads on the first semiconductor chip to a first

plurality of bond pads on the second semiconductor chip.

8. The package of claim 7, Haba et al. show wherein the plurality of bonds pads on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second semiconductor chip corresponding to the edge of the first semiconductor chip.

16. The package of claim 1, Haba et al. further comprising: a third semiconductor chip **910c** stacked offset over the second semiconductor chip such that a portion of the second semiconductor chip is exposed; and a fourth semiconductor chip **910d** stacked offset over the third semiconductor chip such that a portion of the third semiconductor chip is exposed; and at least one first conductor electrically connecting the exposed portions of the first, second and third semiconductor chips to the fourth semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip.

17. The package of claim 16, Haba et al. show wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first, second and third semiconductor chips to a first plurality of bonding pads on the fourth semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

19. The package of claim 1, Haba et al. show wherein the first and second semiconductor chips are a same type of chip.

21. Haba et al. (figures 1 to 14) specifically figure 9 show a method for fabricating a stacked semiconductor package **900**, comprising: forming a stacked chip package including at least a first semiconductor chip **910a** and a second semiconductor chip **910b** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; and electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor **(wire electrically connecting 910a to 910b but not labeled)** such that the conductor does not extend beyond a periphery of the first semiconductor chip.

Claims 1 to 15 and 19 to 22 are rejected under 35 U.S.C. § 102(e) as being anticipated by Brooks (U.S. Patent Application Publication # 2003/0153122 A1).

1. Brooks (figures 1 to 4) specifically figures 2 and 4 show a stacked semiconductor package comprising: a first semiconductor chip **204**; a second semiconductor chip **206** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; and at least one first conductor **220** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip.

2. The package of claim 1, Brooks show wherein the first conductor electrically connects at least one bond pad on the first semiconductor chip with at least one bond pad on the second semiconductor chip.

3. The package of claim 2, Brooks further comprising: a redistribution pattern **213** electrically connecting the bond pad on the second semiconductor chip to a differently positioned bond pad on the second semiconductor chip.

4. The package of claim 3, Brooks further comprising: a frame supporting **202** a chip package structure, the chip package structure including at least the first and second semiconductor

chips; and at least one second conductor **224** electrically connecting the differently positioned bond pad to the frame.

5. The package of claim 4, Brooks show wherein the second conductor electrically connects the differently positioned bond pad to a bond pad on the frame.

6. The package of claim 1, Brooks show wherein a plurality of first conductors **220** electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Brooks further comprising: the plurality of first conductors respectively electrically connecting a plurality of bond pads **210** on the first semiconductor chip to a first plurality of bond pads on the second semiconductor chip **212**.

8. The package of claim 7, Brooks show wherein the plurality of bonds pads on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second semiconductor chip corresponding to the edge of the first semiconductor chip.

9. The package of claim 8, Brooks further comprising: a redistribution pattern **213** electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip, the second plurality of bond pads arranged adjacent to a different edge of the second semiconductor chip.

10. The package of claim 7, Brooks further comprising: a redistribution pattern **213** electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip.

11. The package of claim 10, Brooks further comprising: a frame **202** supporting a chip package structure, the chip package structure including at least the first and second semiconductor chips **204,206**; and a plurality of second conductors **224** electrically connecting the second plurality of bond pads on the second semiconductor chip to the frame.

12. The package of claim 11, Brooks show wherein the frame is one of a printed circuit board and a flexible substrate.

13. The package of claim 11, Brooks show wherein the frame includes a die pad portion **324** supporting the chip package structure and an inner lead portion **224** to which the plurality of second conductors are electrically connected.

14. The package of claim 13, Brooks further comprising: a sealing resin (inherent) sealing the first and second semiconductor chips, the redistribution pattern, the first and second plurality of conductors, and a portion of the frame.

15. The package of claim 11, Brooks show wherein the plurality of first and second conductors **220,222,224** are bonding wires.

19. The package of claim 1, wherein the first and second semiconductor chips are a same type of chip.

20. Brooks (figures 1 to 4) specifically figures 2 and 4 show a stacked semiconductor package comprising: a stacked chip structure including an upper semiconductor chip **206** and at least one lower semiconductor chip **204** disposed under at least a portion of the upper semiconductor chip; and a redistribution pattern **213** redistributing a first plurality of bond pads **212** on the upper semiconductor chip to a differently positioned second plurality of bond pads on the upper semiconductor chip, the first plurality of bond pads **210** being electrically connected with the lower semiconductor chip.

21. Brooks (figures 1 to 4) specifically figures 2 and 4 show a method for fabricating a stacked semiconductor package, comprising: forming a stacked chip package including at least a first semiconductor chip **204** and a second semiconductor chip **206** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; and electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor **220** such that the conductor does not extend beyond a periphery of the first semiconductor chip.

22. Brooks (figures 1 to 4) specifically figures 2 and 4 show a method for fabricating a stacked semiconductor package, comprising: forming a stacked chip structure including an upper semiconductor chip **206** and at least one lower semiconductor chip

204 disposed under at least a portion of the upper semiconductor chip; and electrically connecting the lower semiconductor chip with a first plurality of bond pads **212** on the upper semiconductor chip; and forming a redistribution pattern **213** redistributing the first plurality of bond pads on the upper semiconductor chip to a differently positioned second plurality of bond pads on the upper semiconductor chip.

Claims 16 to 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Brooks (U.S. Patent Application Publication # 2003/0153122 A1) in view of Haba et al. (U.S. Patent # 6,376,904 B1).

Brooks show the features of the claimed invention as detailed invention, particularly show a third semiconductor chip **208** stacked offset over the second semiconductor chip such that a portion of the second semiconductor chip is exposed. Brooks fails to explicitly show a fourth semiconductor chip stacked offset over the third semiconductor chip such that a portion of the third semiconductor chip is exposed; and at least one first conductor electrically connecting the exposed portions of the first, second and third semiconductor chips to the fourth semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip.

Haba et al. is cited for showing a redistributed bond pads in stacked integrated circuit die package. Specifically Brooks (figures 1 to 4) specifically figures 2 and 4 show a forth semiconductor chip for the purpose of providing connectivity between bond pads on the package substrate and metal circuitry.

17. The package of claim 16, the combination showing wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first, second and third semiconductor chips to a first plurality of bonding pads on the fourth semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

18. The package of claim 17, the combination show further comprising: a redistribution pattern electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip.

Therefore, it would have been obvious to one of ordinary skill in the art to use Haba et al.'s forth semiconductor chip to modify Brooks' stack of semiconductor chips for the purpose `providing connectivity between bond pads on the package substrate and metal circuitry.`

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,784,786,787,773,696,698	6/24/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,784,786,787,773,696,698	6/24/05
Electronic data base(s): U.S. Patents EAST	6/24/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/25/05